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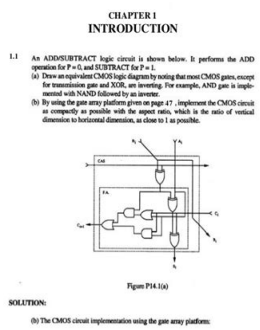

CHAPTER 1
INTRODUCTION

1.1 An ADD/SUBTRACT logic circuit is shown below. It performs the ADD operation for P = 0, and SUBTRACT for P = 1.
(a) Draw an equivalent CMOS logic diagram by noting that most CMOS gates, except for transmission gate and XOR, are inverting. For example, AND gate is implemented with NAND followed by an inverter.
(b) By using the gate array platform given on page 47 , implement the CMOS circuit as compactly as possible with the aspect ratio, which is the ratio of vertical dimension to horizontal dimension, as close to 1 as possible.

Figure P14.1(a)

SOLUTION:

(b) The CMOS circuit implementation using the gate array platform:

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